International
IOR Rectifier

Data Sheet No. PD60019 Rev.P

IR2130/IR2132(J)(S) & (PbF)

3-PHASE BRIDGE DRIVER

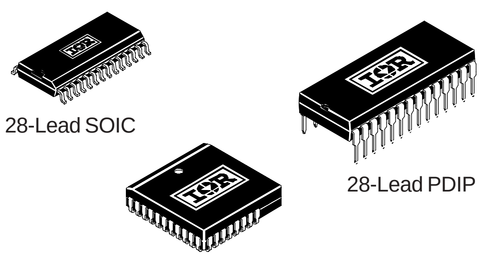
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Also available LEAD-FREE

Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	675 & 425 ns
Deadtime (typ.)	2.5 µs (IR2130) 0.8 µs (IR2132)

Packages



28-Lead SOIC

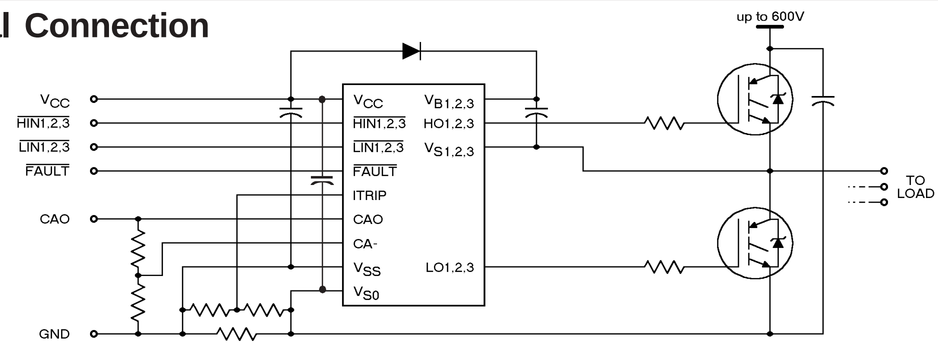
28-Lead PDIP

44-Lead PLCC w/o 12 Leads

Description

The IR2130/IR2132(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain $\overline{FAULT}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0}. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage		-0.3	625	
$V_{S1,2,3}$	High Side Floating Offset Voltage		$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V
$V_{HO1,2,3}$	High Side Floating Output Voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage		-0.3	25	
V_{SS}	Logic Ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)		V_{SS} - 0.3	(V_{SS} + 15) or (V_{CC} + 0.3) whichever is lower	
V_{FLT}	$\overline{FAULT}$ Output Voltage		V_{SS} - 0.3	V_{CC} + 0.3	
V_{CAO}	Operational Amplifier Output Voltage		V_{SS} - 0.3	V_{CC} + 0.3	
V_{CA-}	Operational Amplifier Inverting Input Voltage		V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
P_D	Package Power Dissipation @ $T_A \le +25°C$	(28 Lead DIP)	—	1.5	W
		(28 Lead SOIC)	—	1.6	
		(44 Lead PLCC)	—	2.0	
Rth_{JA}	Thermal Resistance, Junction to Ambient	(28 Lead DIP)	—	83	°C/W
		(28 Lead SOIC)	—	78	
		(44 Lead PLCC)	—	63	
T_J	Junction Temperature		—	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0}. The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	V_{SS} + 5	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	V_{SS} + 5	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of (V_{S0} - 5V) to (V_{S0} + 600V). Logic state held for V_S of (V_{S0} - 5V) to (V_{S0} - V_{BS}). (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS}, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	11	500	675	850	ns	
t_{off}	Turn-Off Propagation Delay	12	300	425	550		V_{IN} = 0 & 5V
t_r	Turn-On Rise Time	13	—	80	125		$V_{S1,2,3}$ = 0 to 600V
t_f	Turn-Off Fall Time	14	—	35	55		
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		V_{IN}, V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	—	400	—		V_{ITRIP} = 1V
t_{flt}	ITRIP to $\overline{\text{FAULT}}$ Indication Delay	16	335	590	845		V_{IN}, V_{ITRIP} = 0 & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time	17	6.0	9.0	12.0	µs	V_{IN}, V_{ITRIP} = 0 & 5V
DT	Deadtime (IR2130)	18	1.3	2.5	3.7		V_{IN} = 0 & 5V
	(IR2132)	18	0.4	0.8	1.2		
SR+	Operational Amplifier Slew Rate (+)	19	4.4	6.2	—	V/µs	
SR-	Operational Amplifier Slew Rate (-)	20	2.4	3.2	—		

NOTE: For high side PWM, HIN pulse width must be ≥ 1.5µsec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{\text{HIN1,2,3}}$ & $\overline{\text{LIN1,2,3}}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

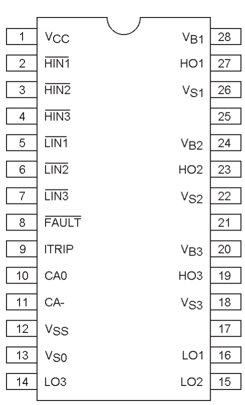
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	21	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	22	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	23	400	490	580	mV	
V_{OH}	High Level Output Voltage, V_{BIAS} - VO	24	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, VO	25	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current	26	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	27	—	15	30		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	28	—	3.0	4.0	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	29	—	450	650	µA	V_{IN} = 0V
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	30	—	225	400		V_{IN} = 5V
I_{ITRIP+}	"High" ITRIP Bias Current	31	—	75	150		ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	32	—	—	100	nA	ITRIP = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	33	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	34	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	35	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	36	8.0	8.7	9.4		
$R_{on,FLT}$	$\overline{\text{FAULT}}$ Low On-Resistance	37	—	55	75	Ω	

Static Electrical Characteristics -- Continued

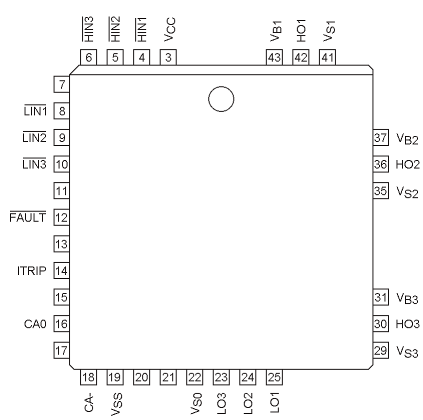
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
I_{O+}	Output High Short Circuit Pulsed Current	38	200	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	39	420	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs
V_{OS}	Operational Amplifer Input Offset Voltage	40	—	—	30	mV	V_{S0} = V_{CA-} = 0.2V
I_{CA-}	CA- Input Bais Current	41	—	—	4.0	nA	V_{CA-} = 2.5V
CMRR	Op. Amp. Common Mode Rejection Ratio	42	60	80	—	dB	V_{S0}=V_{CA-}=0.1V & 5V
PSRR	Op. Amp. Power Supply Rejection Ratio	43	55	75	—		V_{S0} = V_{CA-} = 0.2V V_{CC} = 10V & 20V
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	44	5.0	5.2	5.4	V	V_{CA-} = 0V, V_{S0} = 1V
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	45	—	—	20	mV	V_{CA-} = 1V, V_{S0} = 0V
$I_{SRC,AMP}$	Op. Amp. Output Source Current	46	2.3	4.0	—	mA	V_{CA-} = 0V, V_{S0} = 1V V_{CAO} = 4V
$I_{SRC,AMP}$	Op. Amp. Output Sink Current	47	1.0	2.1	—		V_{CA-} = 1V, V_{S0} = 0V V_{CAO} = 2V
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	48	—	4.5	6.5		V_{CA-} = 0V, V_{S0} = 5V V_{CAO} = 0V
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	49	—	3.2	5.2		V_{CA-} = 5V, V_{S0} = 0V V_{CAO} = 5V

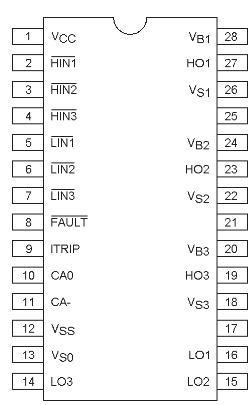
Lead Assignments



28 Lead PDIP



44 Lead PLCC w/o 12 Leads

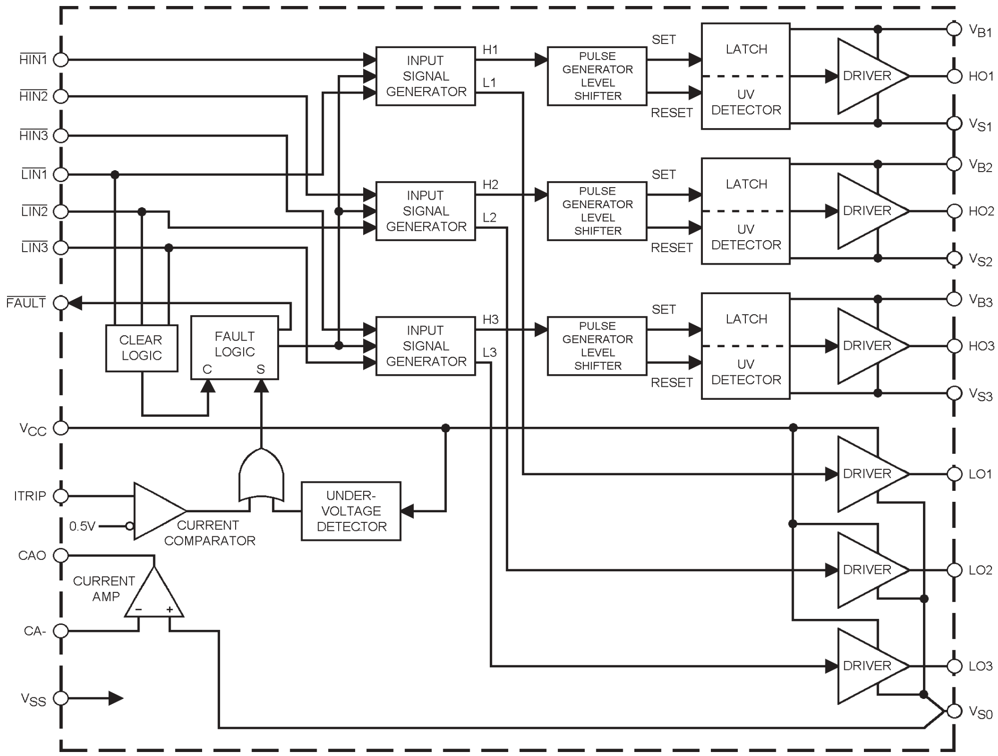


28 Lead SOIC (Wide Body)

IR2130 / IR2132	IR2130J / IR2132J	IR2130S / IR2132S

Part Number

Functional Block Diagram



Lead Definitions

Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
V_{S0}	Low side return and positive input of current amplifier

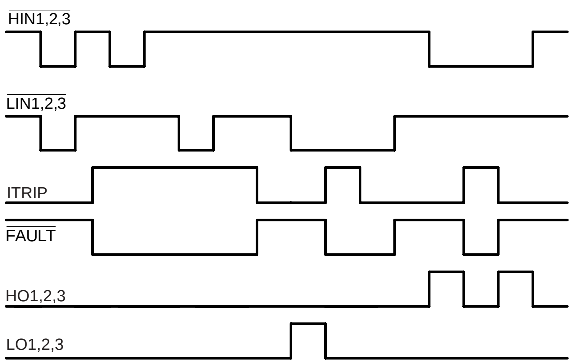


Figure 1. Input/Output Timing Diagram

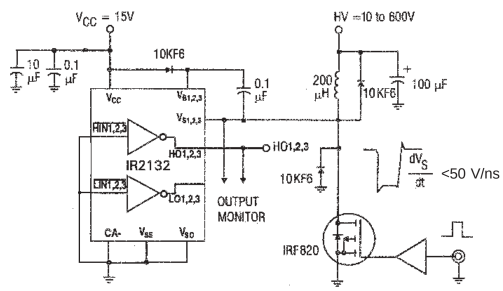


Figure 2. Floating Supply Voltage Transient Test Circuit

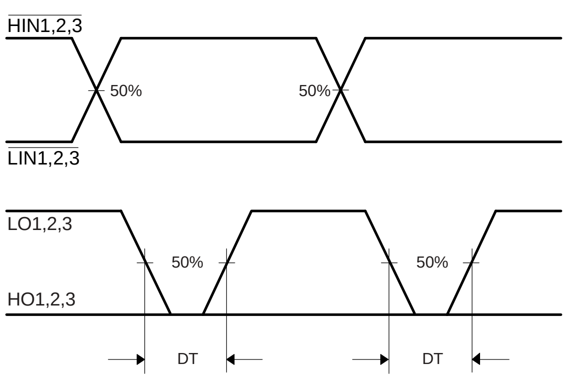


Figure 3. Deadtime Waveform Definitions

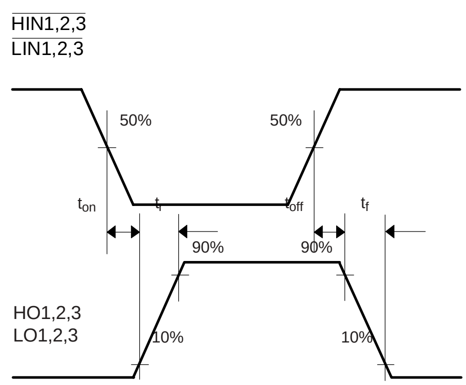


Figure 4. Input/Output Switching Time Waveform Definitions

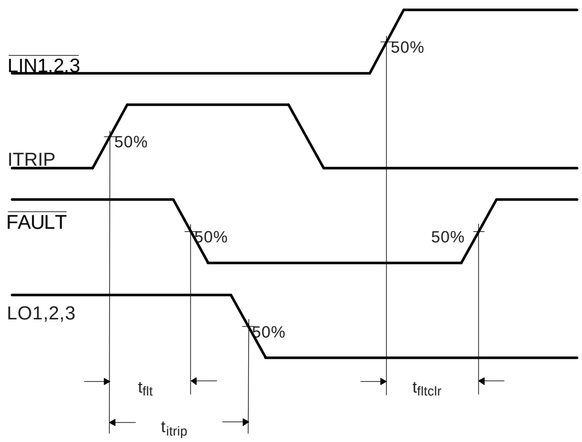


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

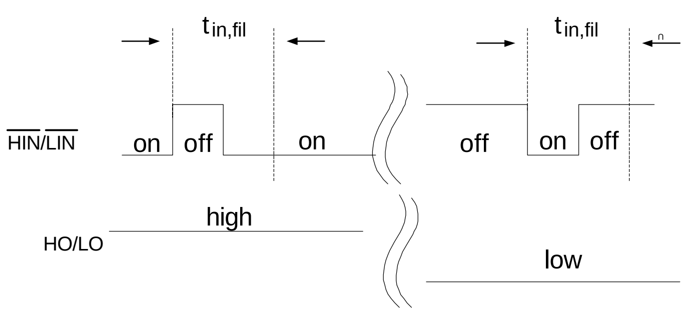


Figure 5.5 Input Filter Function

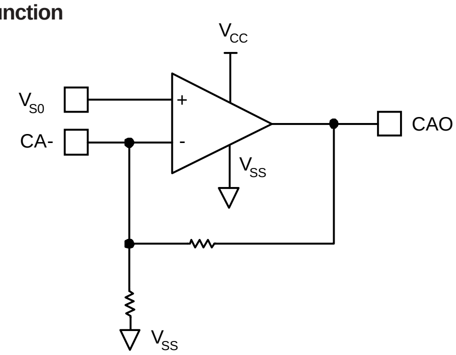
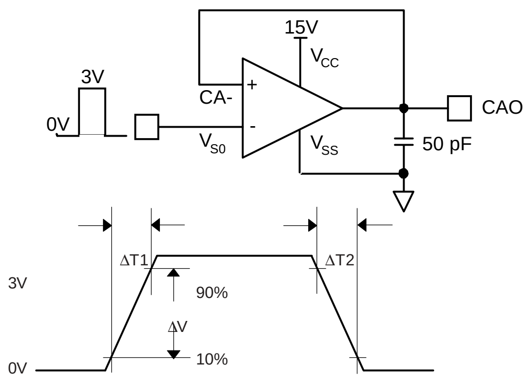
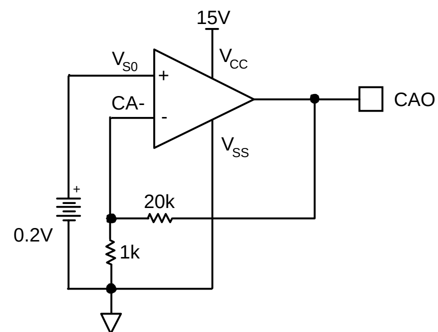


Figure 6. Diagnostic Feedback Operational Amplifier Circuit



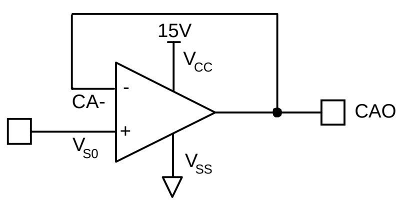
$$SR+ = \frac{\Delta V}{\Delta T1} \qquad SR- = \frac{\Delta V}{\Delta T2}$$

Figure 7. Operational Amplifier Slew Rate Measurement



$$V_{OS} = \frac{V_{CAO}}{21} - 0.2V$$

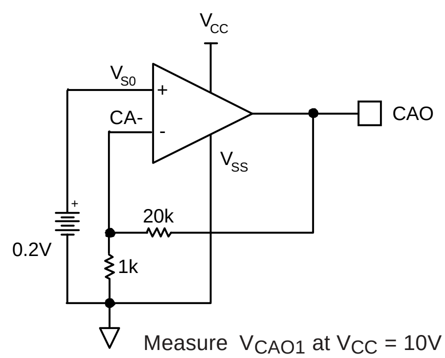
Figure 8. Operational Amplifier Input Offset Voltage Measurement



Measure V_{CAO1} at V_{S0} = 0.1V
V_{CAO2} at V_{S0} = 5V

$$CMRR = -20 * LOG \left| \frac{(V_{CAO1}-0.1V) - (V_{CAO2}-5V)}{4.9V} \right| (dB)$$

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements



Measure V_{CAO1} at V_{CC} = 10V
V_{CAO2} at V_{CC} = 20V

$$PSRR = -20 * LOG \left| \frac{V_{CAO1} - V_{CAO2}}{(10V)\ (21)} \right|$$

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

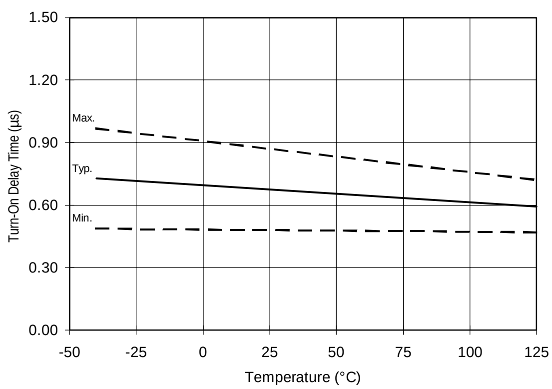


Figure 11A. Turn-On Time vs. Temperature

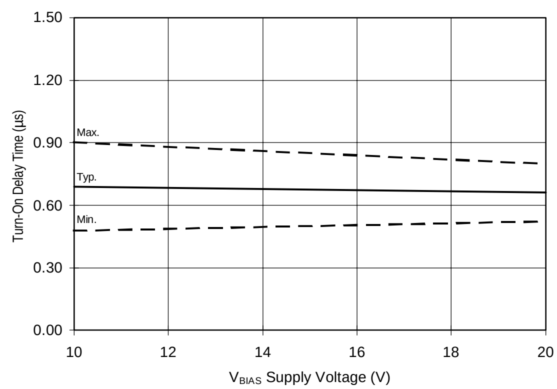


Figure 11B. Turn-On Time vs. Supply Voltage

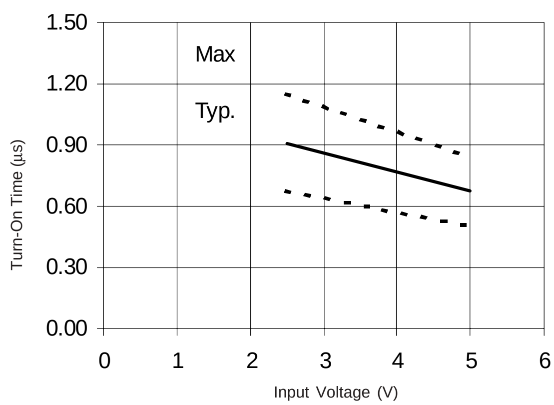


Figure 11C. Turn-On Time vs. Voltage

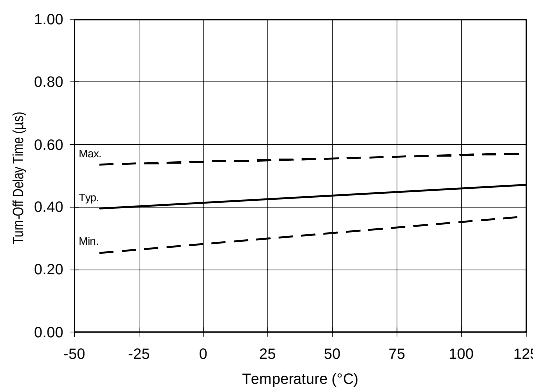


Figure 12A. Turn-Off Time vs. Temperature

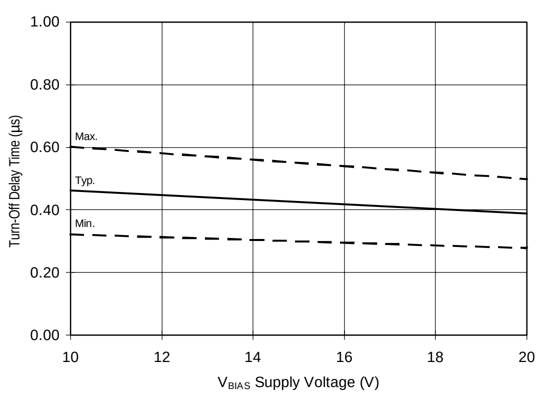


Figure 12B. Turn-Off Time vs. Supply Voltage

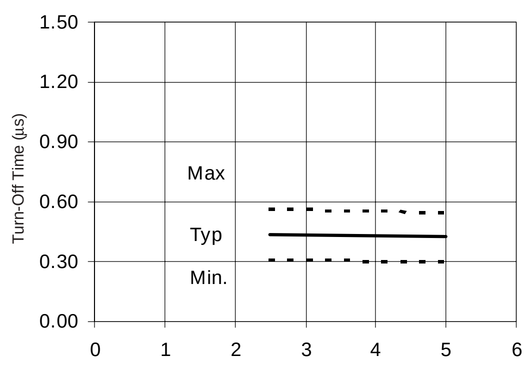


Figure 12C. Turn-Off Time vs. Input Voltage

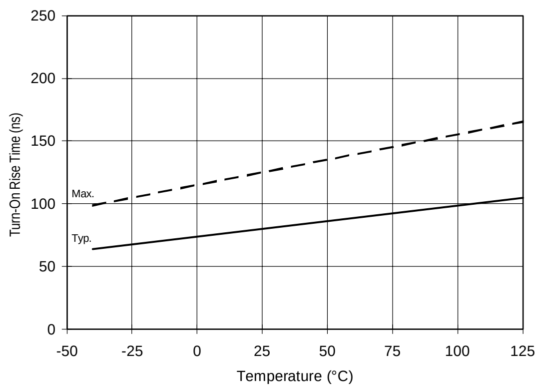


Figure 13A. Turn-On Rise Time vs. Temperature

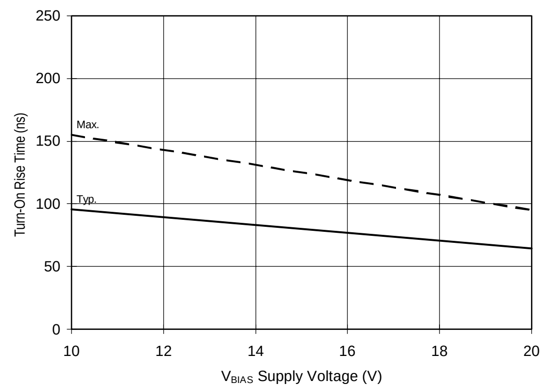


Figure 13B. Turn-On Rise Time vs. Voltage

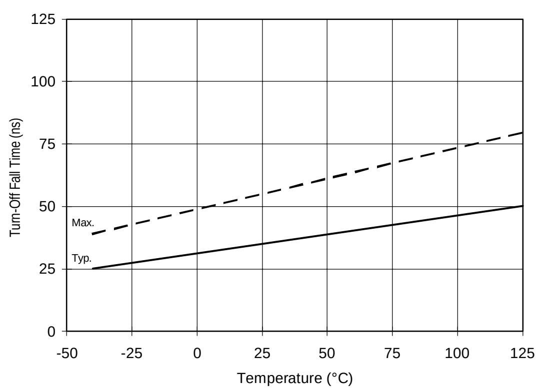


Figure 14A. Turn-Off Fall Time vs. Temperature

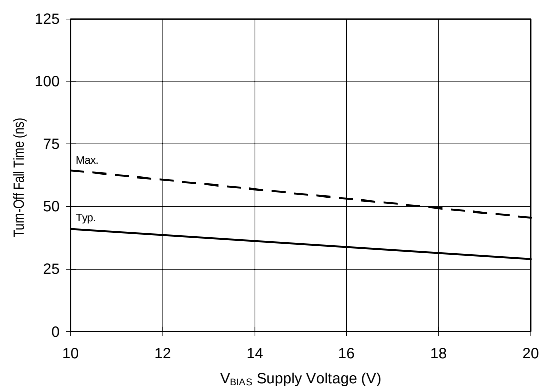


Figure 14B. Turn-Off Fall Time vs. Voltage

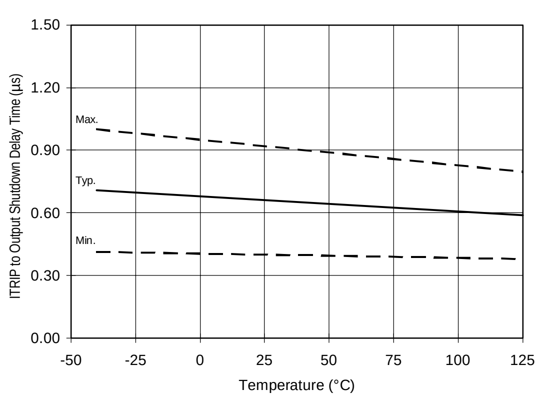


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

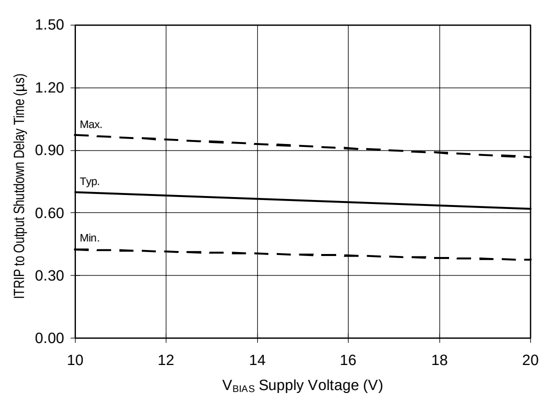


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

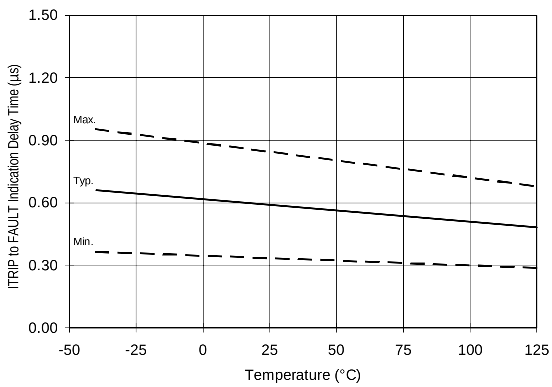


Figure 16A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

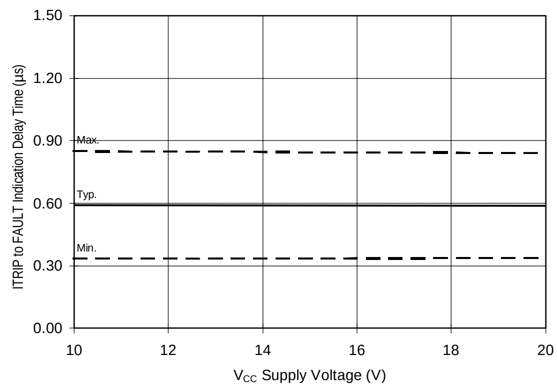


Figure 16B. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Voltage

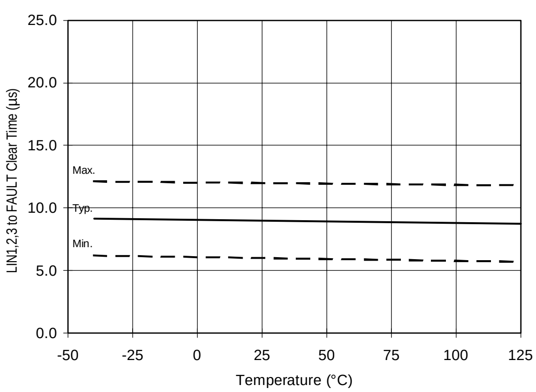


Figure 17A. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Temperature

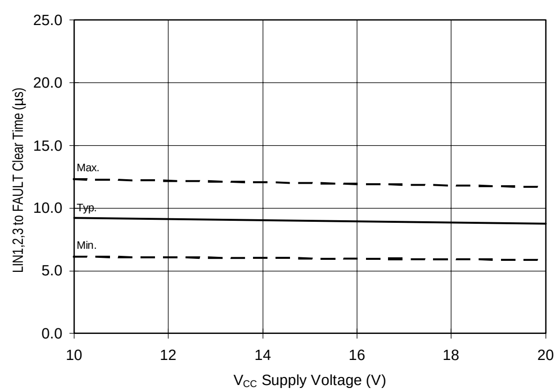


Figure 17B. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Voltage

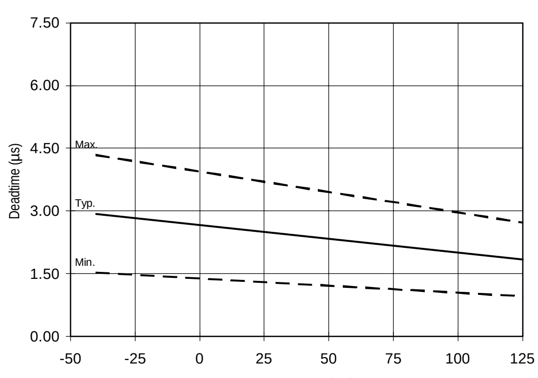


Figure 18A. Deadtime vs. Temperature (IR2130)

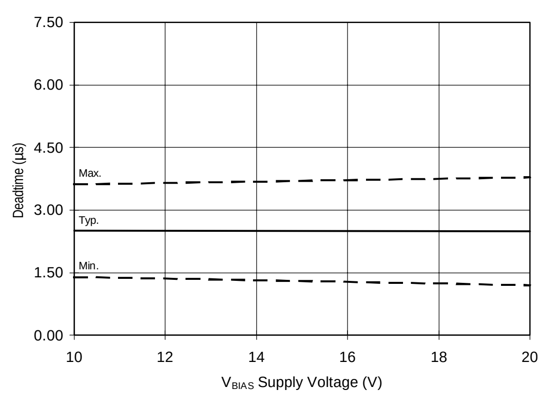


Figure 18B. Deadtime vs. Voltage (IR2130)

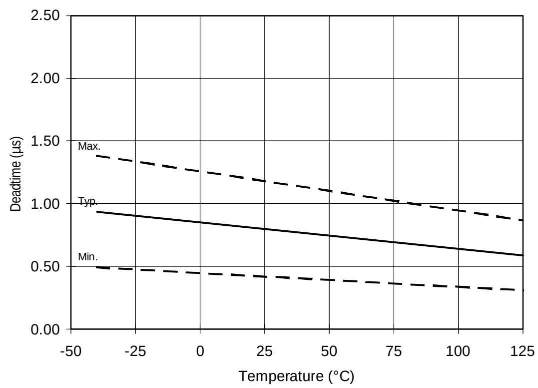


Figure 18C. Deadtime vs. Temperature (IR2132)

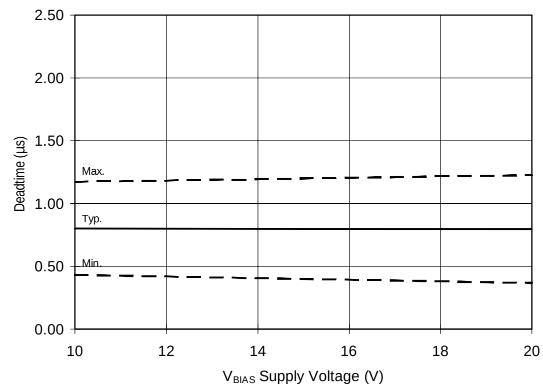


Figure 18D. Deadtime vs. Voltage (IR2132)

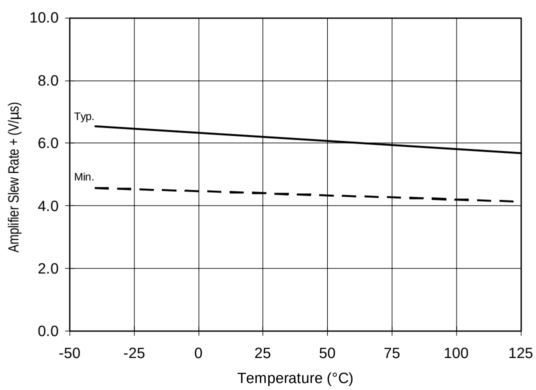


Figure 19A. Amplifier Slew Rate (+) vs. Temperature

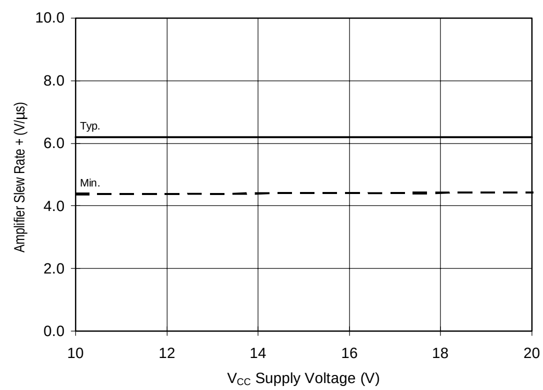


Figure 19B. Amplifier Slew Rate (+) vs. Voltage

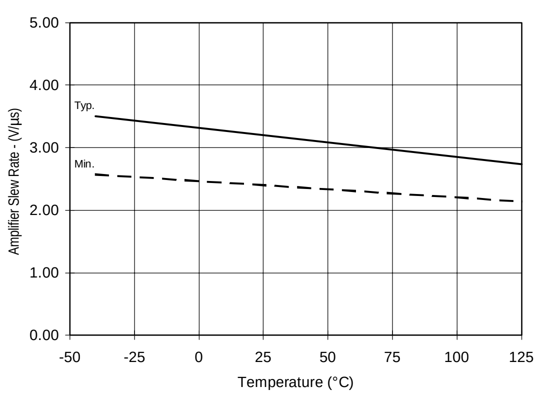


Figure 20A. Amplifier Slew Rate (-) vs. Temperature

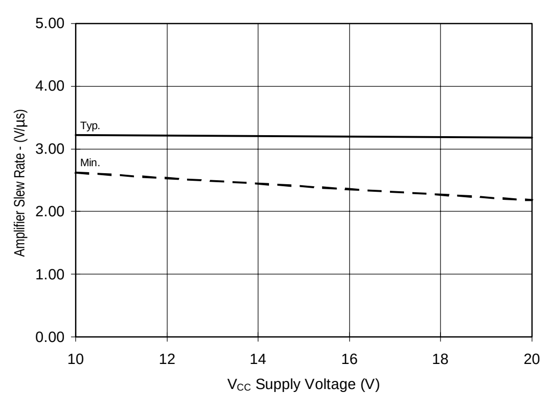


Figure 20B. Amplifier Slew Rate (-) vs. Voltage

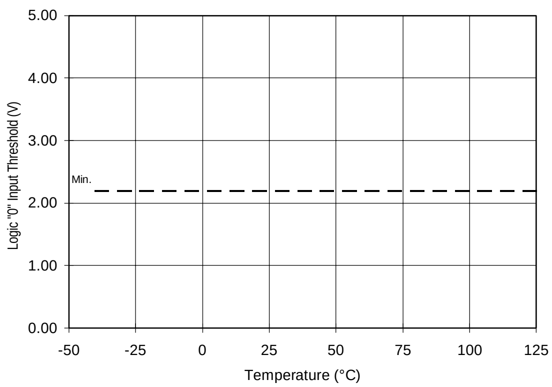


Figure 21A. Logic “0” Input Threshold vs. Temperature

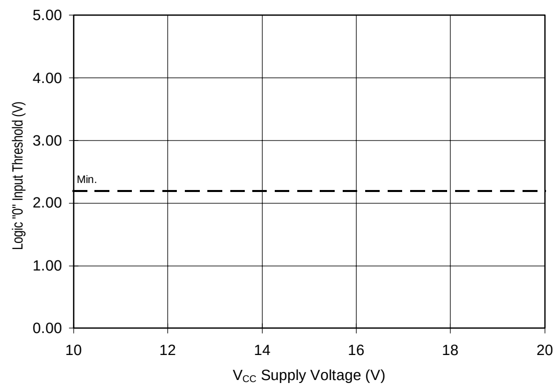


Figure 20B. Logic “0” Input Threshold vs. Voltage

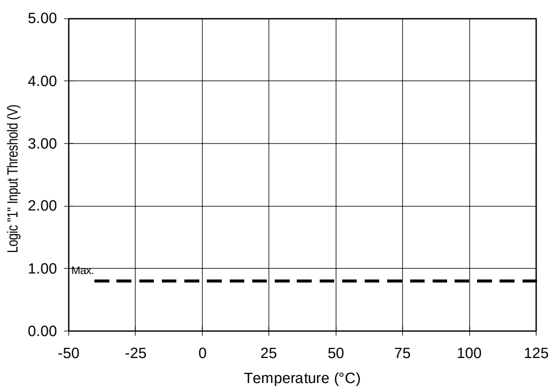


Figure 22A. Logic “1” Input Threshold vs. Temperature

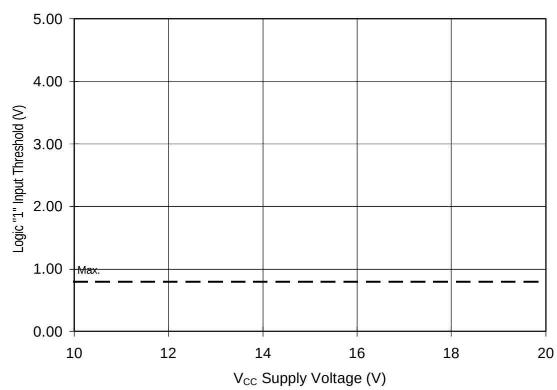


Figure 22B. Logic “1” Input Threshold vs. Voltage

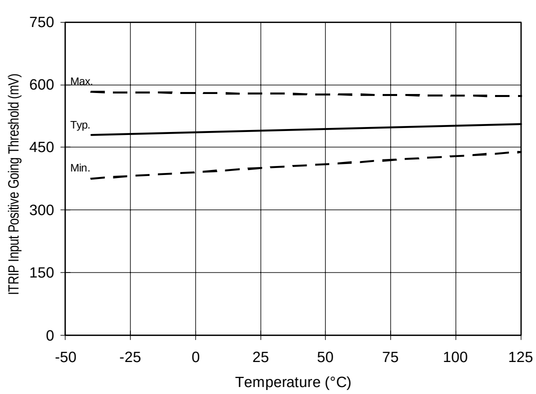


Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

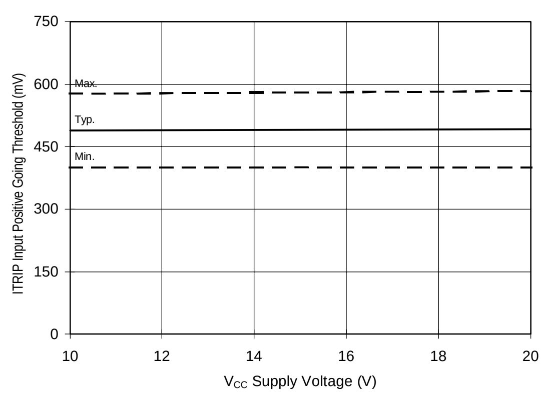


Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

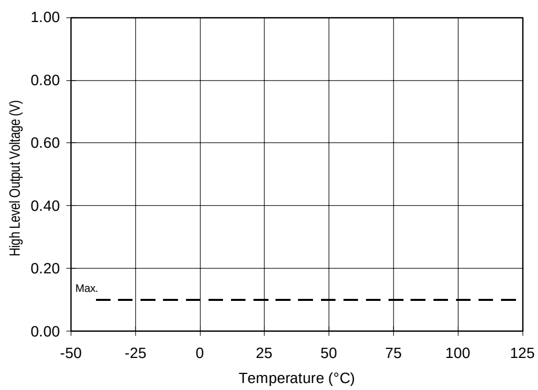


Figure 24A. High Level Output vs. Temperature

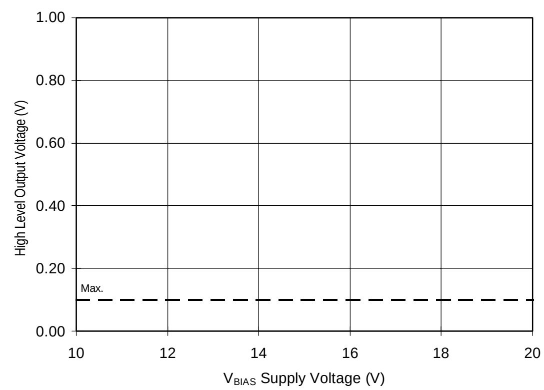


Figure 24B. High Level Output vs. Voltage

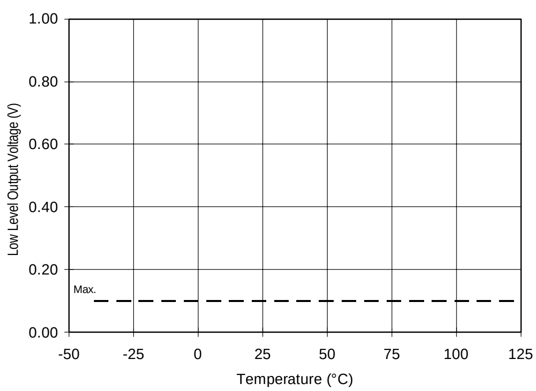


Figure 25A. Low Level Output vs. Temperature

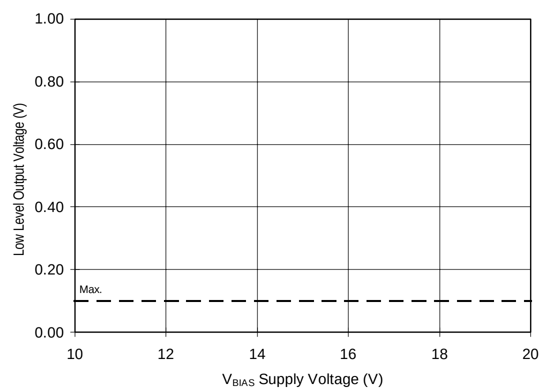


Figure 25B. Low Level Output vs. Voltage

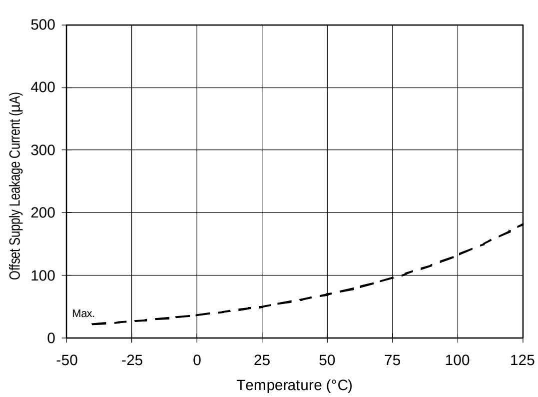


Figure 26A. Offset Supply Leakage Current vs. Temperature

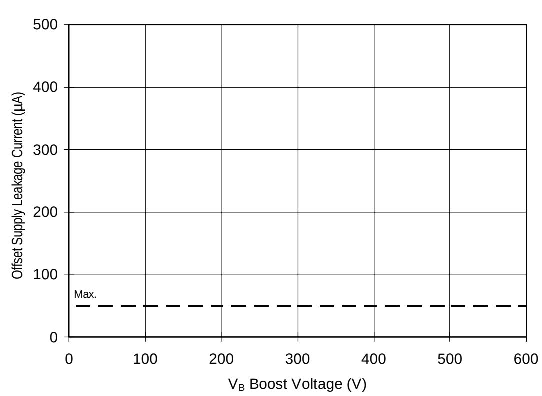


Figure 26B. Offset Supply Leakage Current vs. Voltage

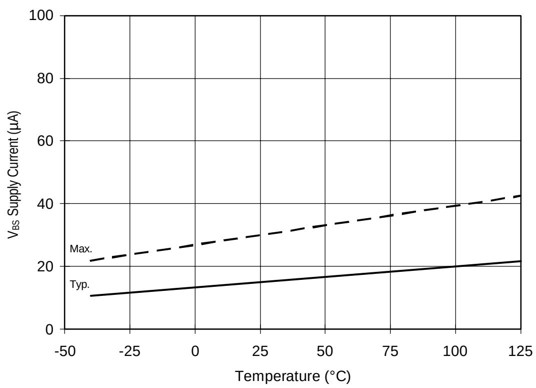


Figure 27A. V_{BS} Supply Current vs. Temperature

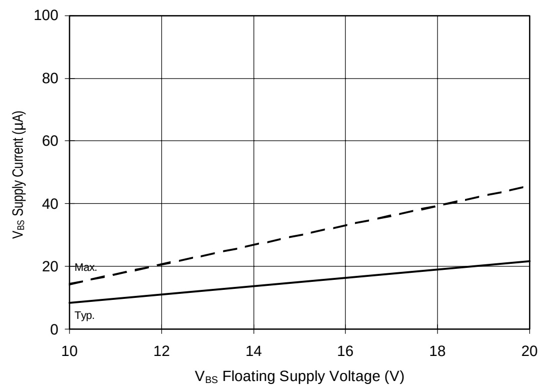


Figure 27B. V_{BS} Supply Current vs. Voltage

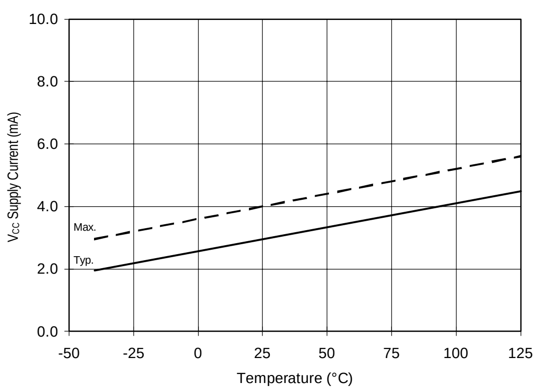


Figure 28A. V_{CC} Supply Current vs. Temperature

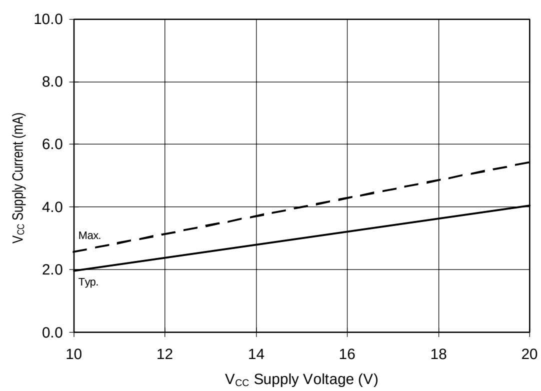


Figure 28B. V_{CC} Supply Current vs. Voltage

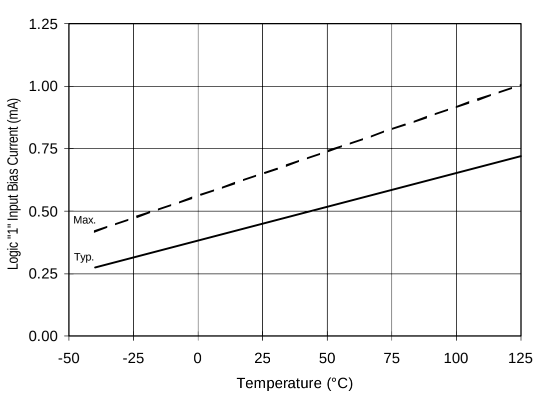


Figure 29A. Logic “1” Input Current vs. Temperature

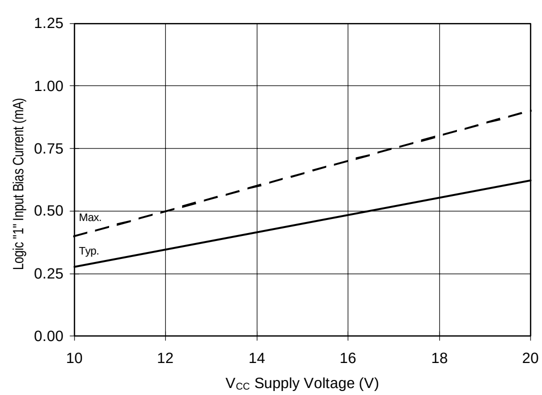


Figure 29A. Logic “1” Input Current vs. Voltage

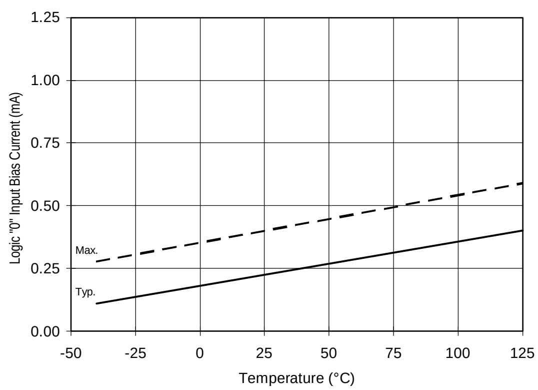


Figure 30A. Logic "0" Input Current vs. Temperature

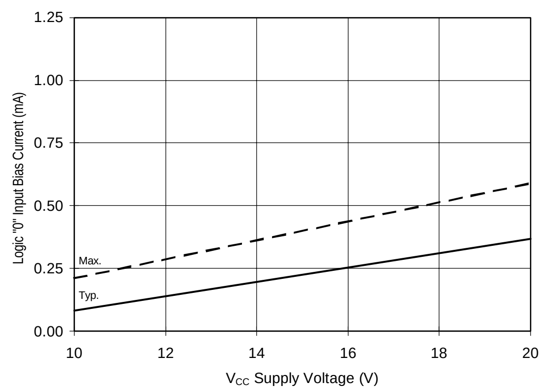


Figure 30B. Logic "0" Input Current vs. Voltage

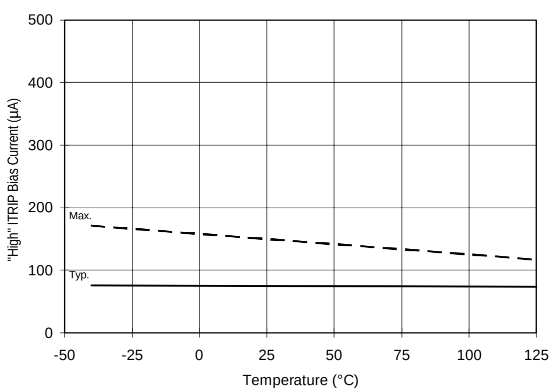


Figure 31A. "High" ITRIP Current vs. Temperature

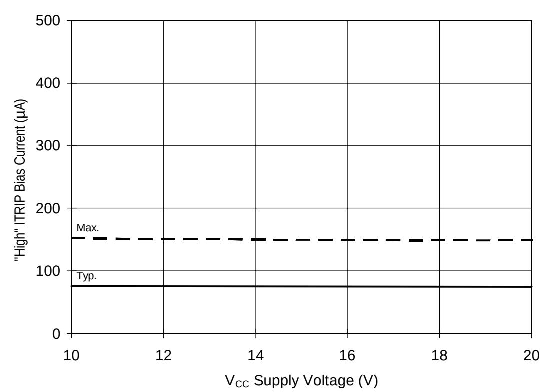


Figure 31B. "High" ITRIP Current vs. Voltage

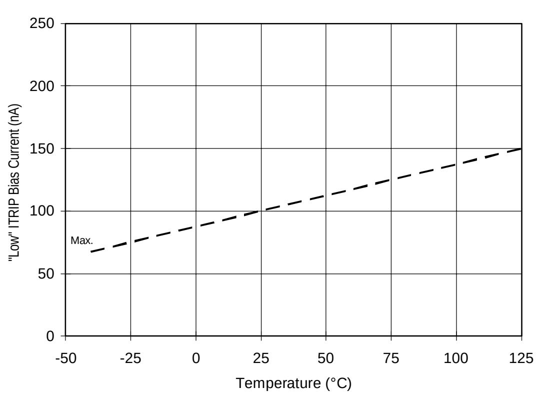


Figure 32A. "Low" ITRIP Current vs. Temperature

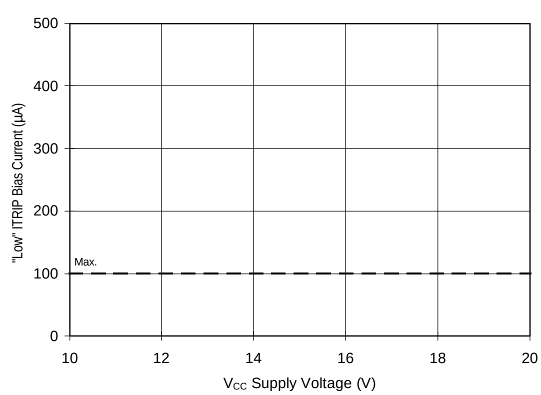


Figure 32B. "Low" ITRIP Current vs. Voltage

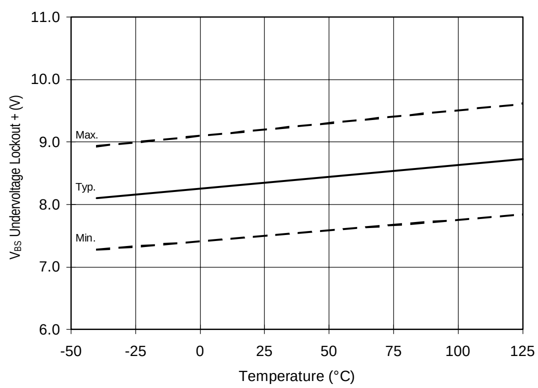


Figure 33. V_{BS} Undervoltage (+) vs. Temperature

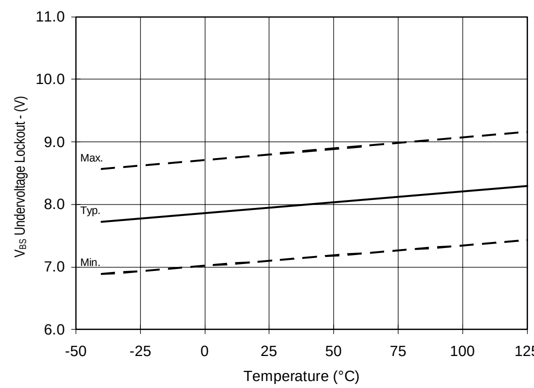


Figure 34. V_{BS} Undervoltage (-) vs. Temperature

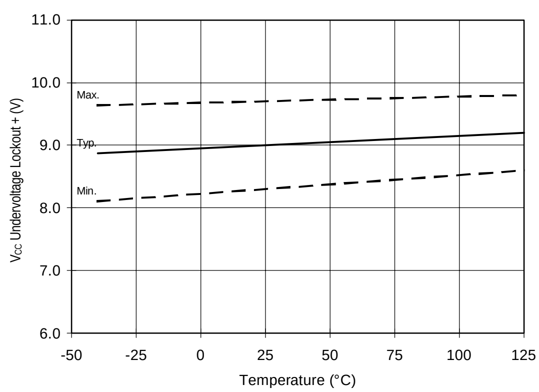


Figure 35. V_{CC} Undervoltage (+) vs. Temperature

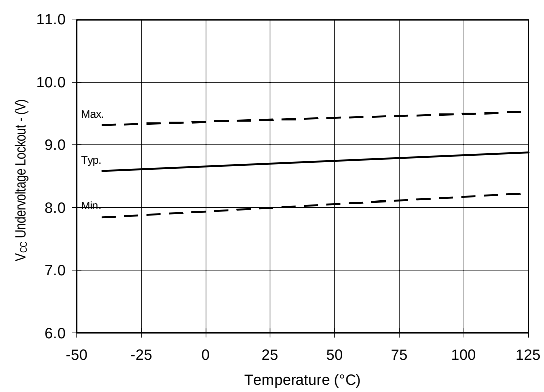


Figure 36. V_{CC} Undervoltage (-) vs. Temperature

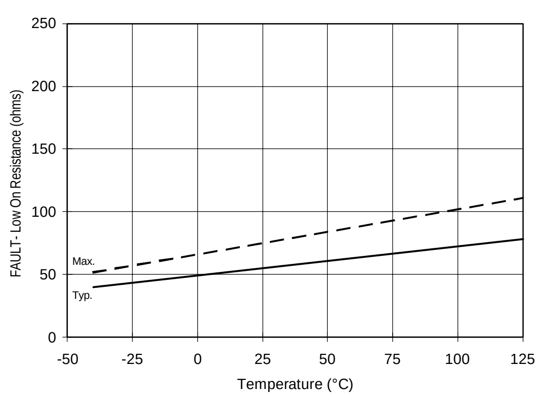


Figure 37A. $\overline{\text{FAULT}}$ Low On Resistance vs. Temperature

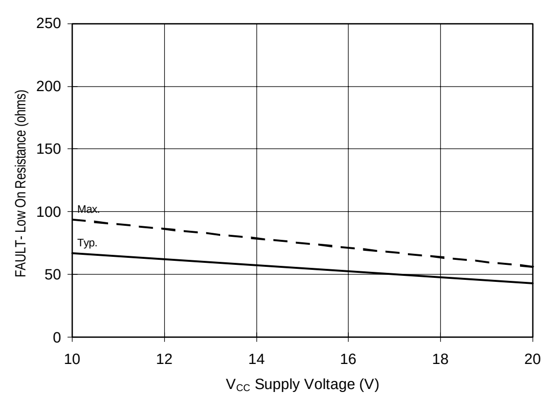


Figure 37B. $\overline{\text{FAULT}}$ Low On Resistance vs. Voltage

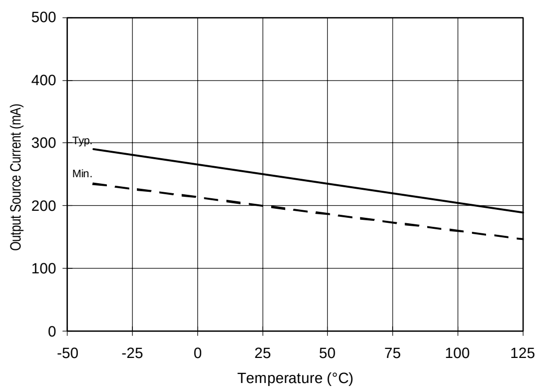


Figure 38A. Output Source Current vs. Temperature

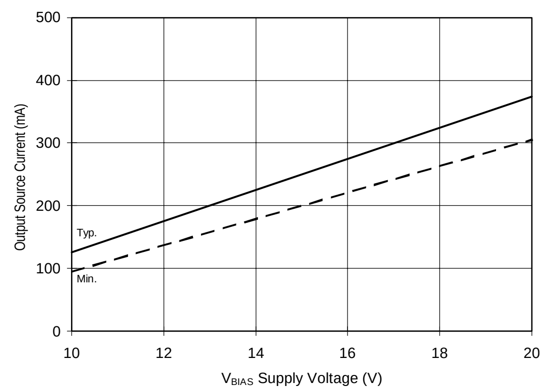


Figure 38B. Output Source Current vs. Voltage

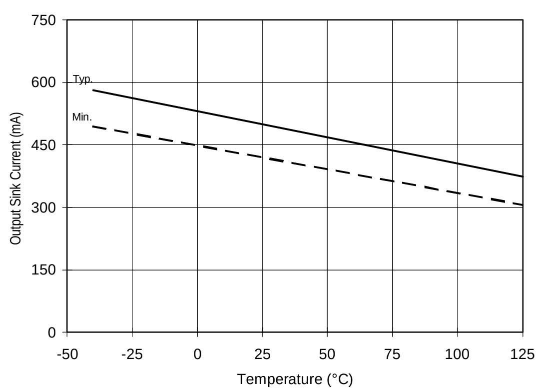


Figure 39A. Output Sink Current vs. Temperature

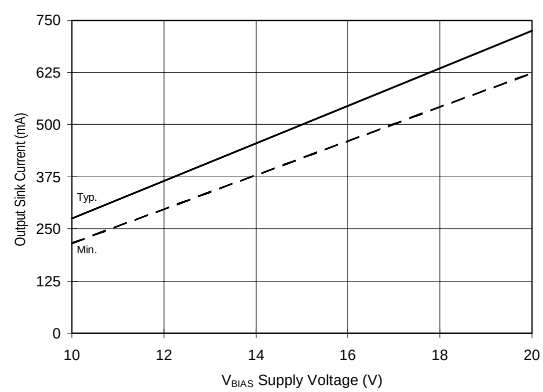


Figure 39B. Output Sink Current vs. Voltage

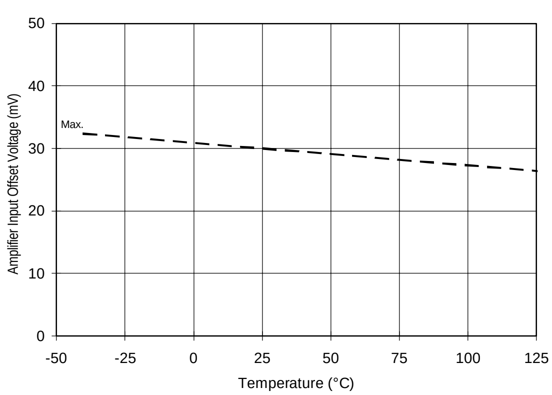


Figure 40A. Amplifier Input Offset vs. Temperature

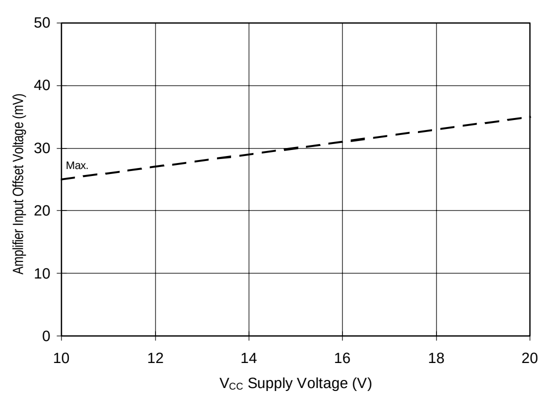


Figure 40B. Amplifier Input Offset vs. Voltage

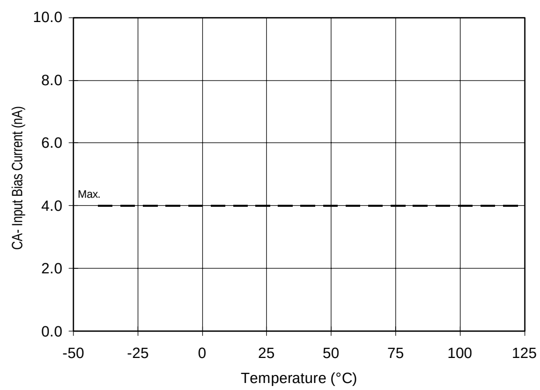


Figure 41A. CA- Input Current vs. Temperature

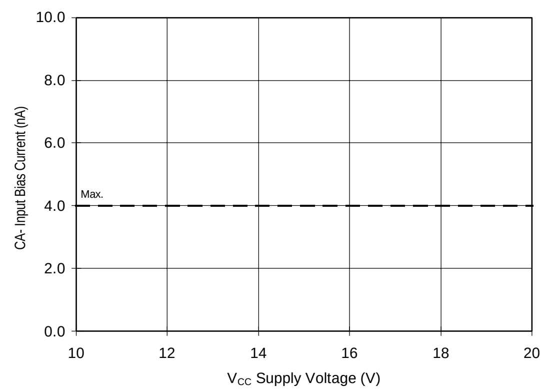


Figure 41B. CA- Input Current vs. Voltage

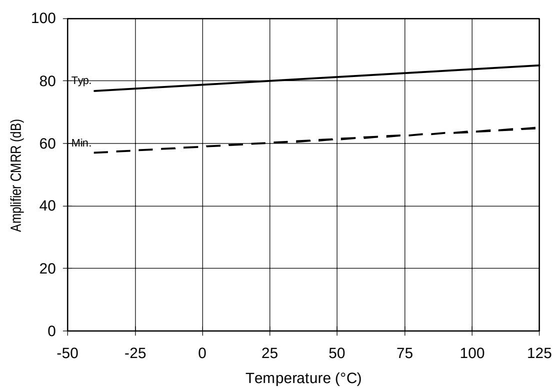


Figure 42A. Amplifier CMRR vs. Temperature

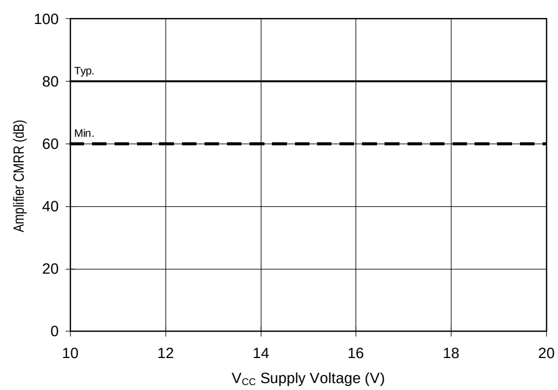


Figure 42B. Amplifier CMRR vs. Voltage

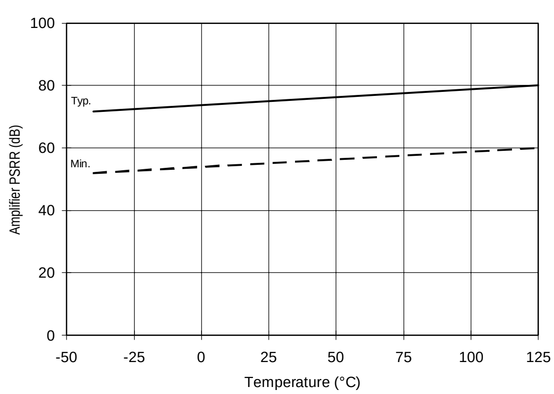


Figure 43A. Amplifier PSRR vs. Temperature

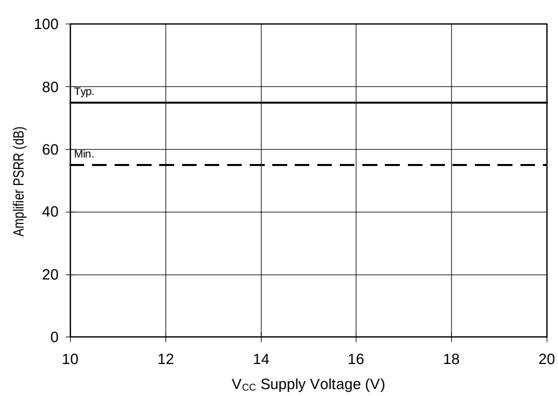


Figure 43B. Amplifier PSRR vs. Voltage

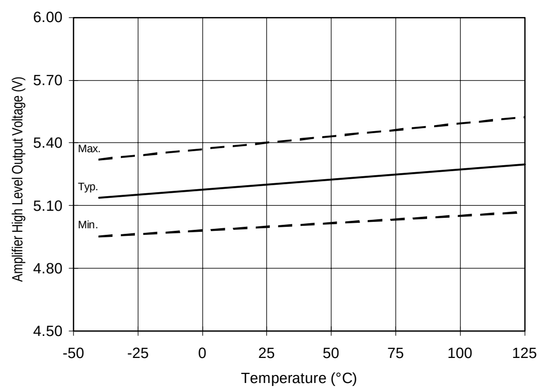


Figure 44A. Amplifier High Level Output vs. Temperature

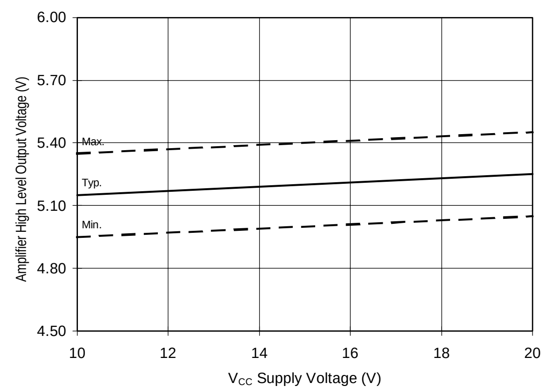


Figure 44B. Amplifier High Level Output vs. Voltage

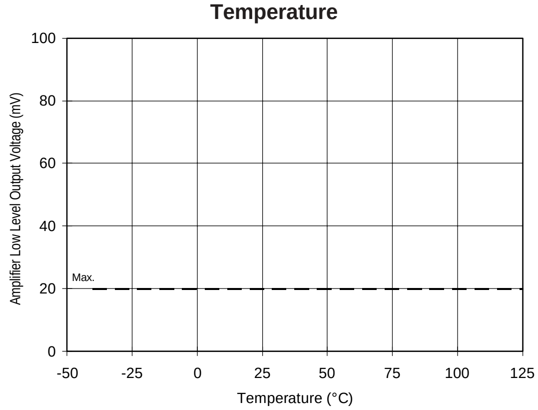


Figure 45A. Amplifier Low Level Output vs. Temperature

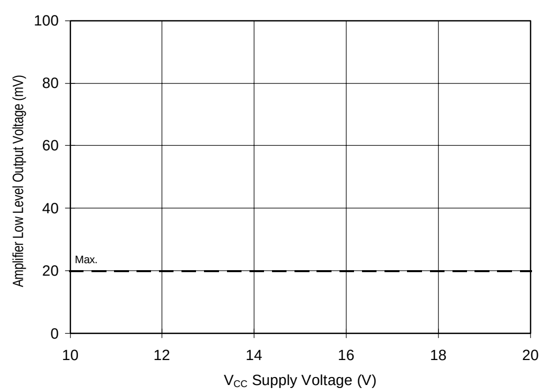


Figure 45B. Amplifier Low Level Output vs. Voltage

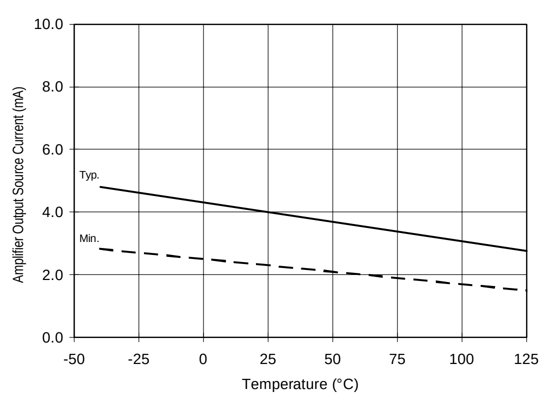


Figure 46A. Amplifier Output Source Current vs. Temperature

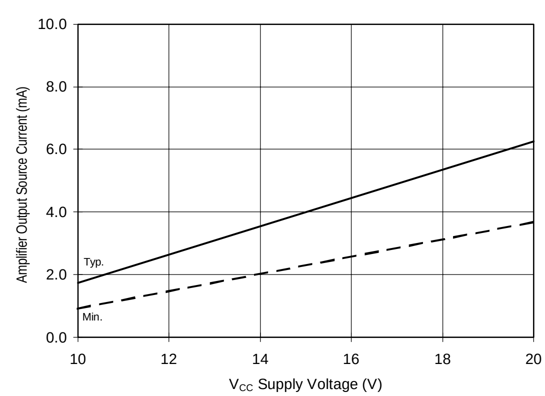


Figure 46B. Amplifier Output Source Current vs. Voltage

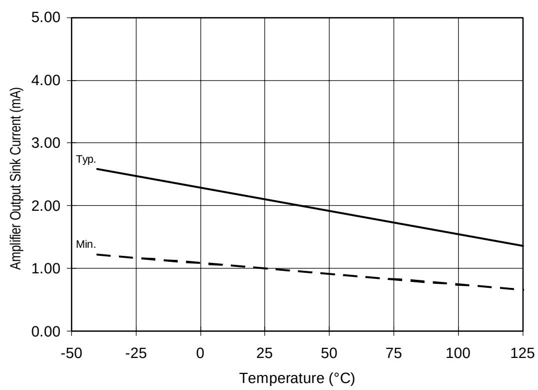


Figure 47A. Amplifier Output Sink Current vs. Temperature

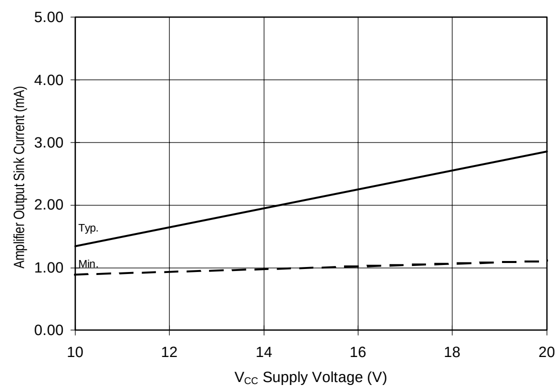


Figure 47B. Amplifier Output Sink Current vs. Voltage

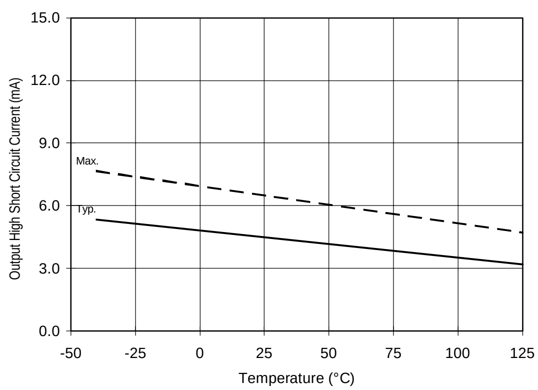


Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

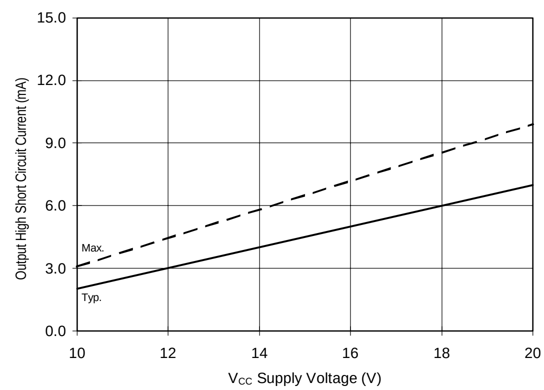


Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

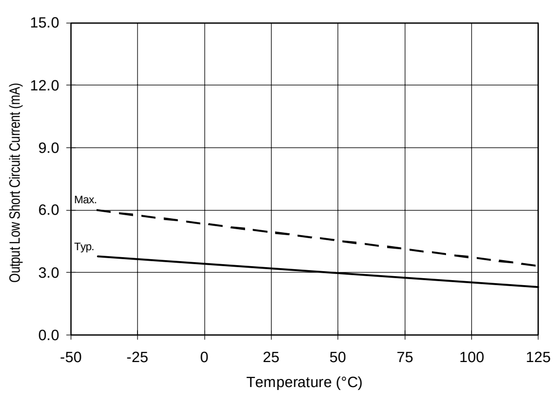


Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

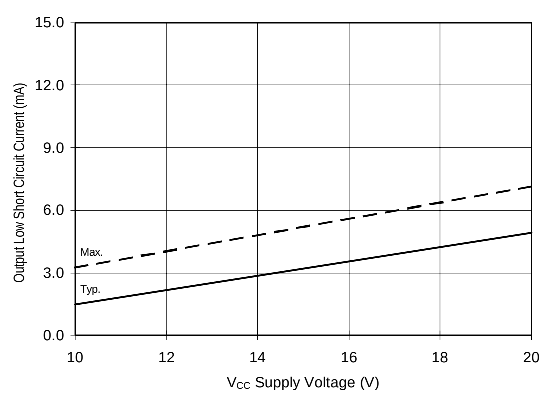


Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

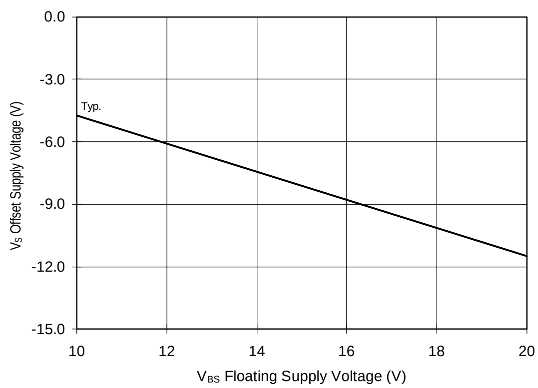


Figure 50. Maximum VS Negative Offset vs. V_{BS} Supply Voltage

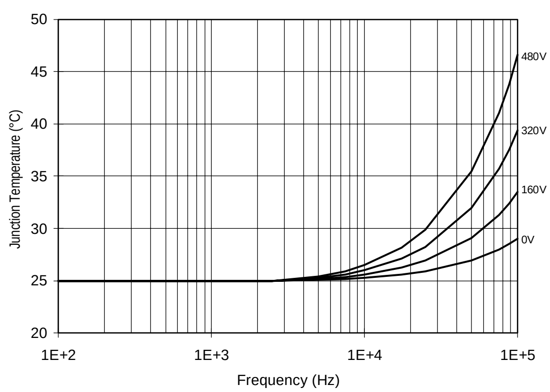


Figure 51. IR2130/IR2132 T_J vs. Frequency (IRF820) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

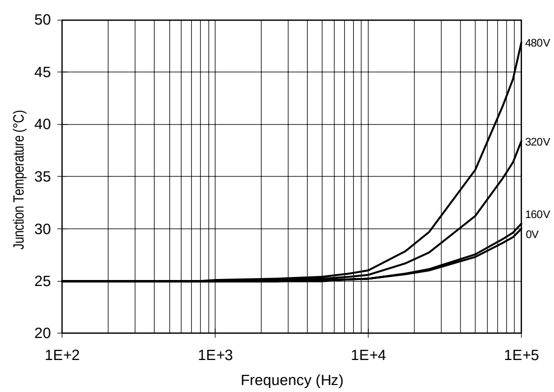


Figure 52. IR2130/IR2132 T_J vs. Frequency (IRF830) $R_{GATE} = 20\Omega$, $V_{CC} = 15V$

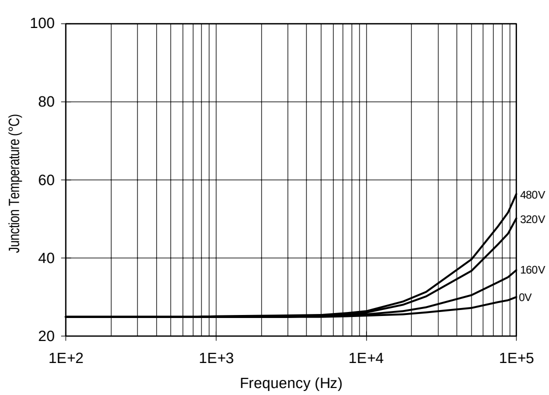


Figure 53. IR2130/IR2132 T_J vs. Frequency (IRF840) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

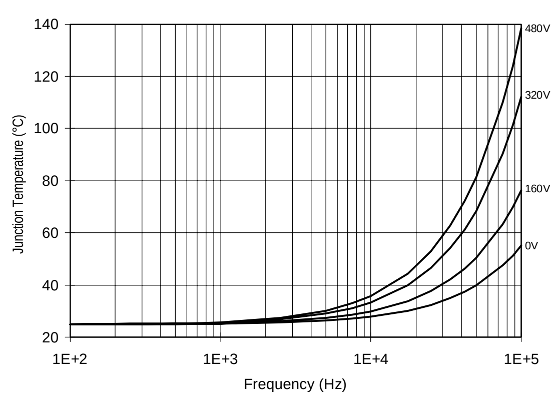


Figure 54. IR2130/IR2132 T_J vs. Frequency (IRF450) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

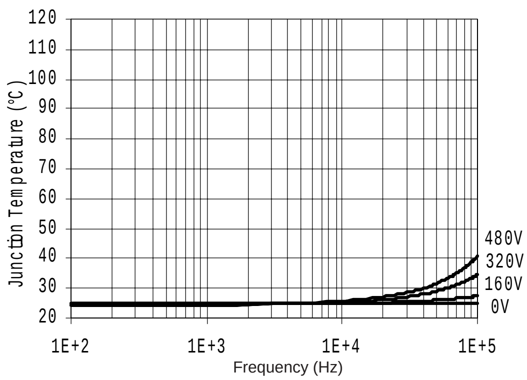


Figure 55. IR2130J/IR2132J
T_J vs. Frequency (IRGPC20KD2)
R_{GATE} = 33Ω, V_{CC} = 15V

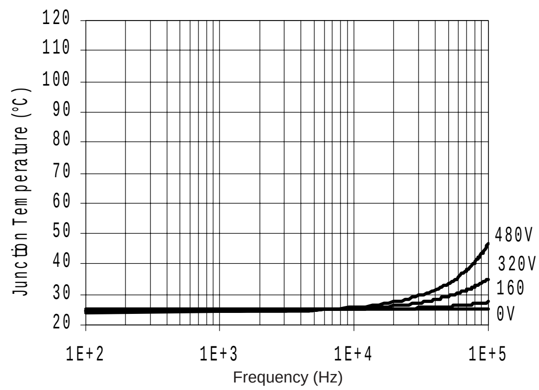


Figure 56. IR2130J/IR2132J
T_J vs. Frequency (IRGPC30KD2)
R_{GATE} = 20Ω, V_{CC} = 15V

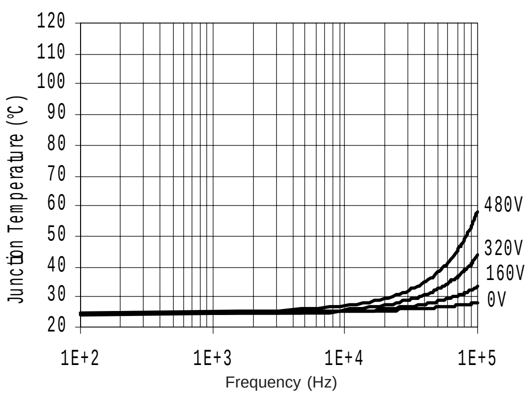


Figure 57. IR2130J/IR2132J
T_J vs. Frequency (IRGPC40KD2)
R_{GATE} = 15Ω, V_{CC} = 15V

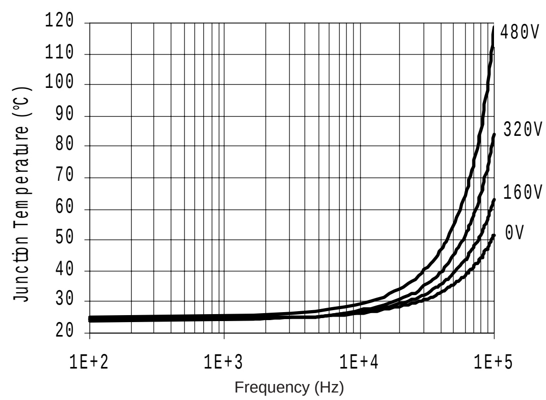
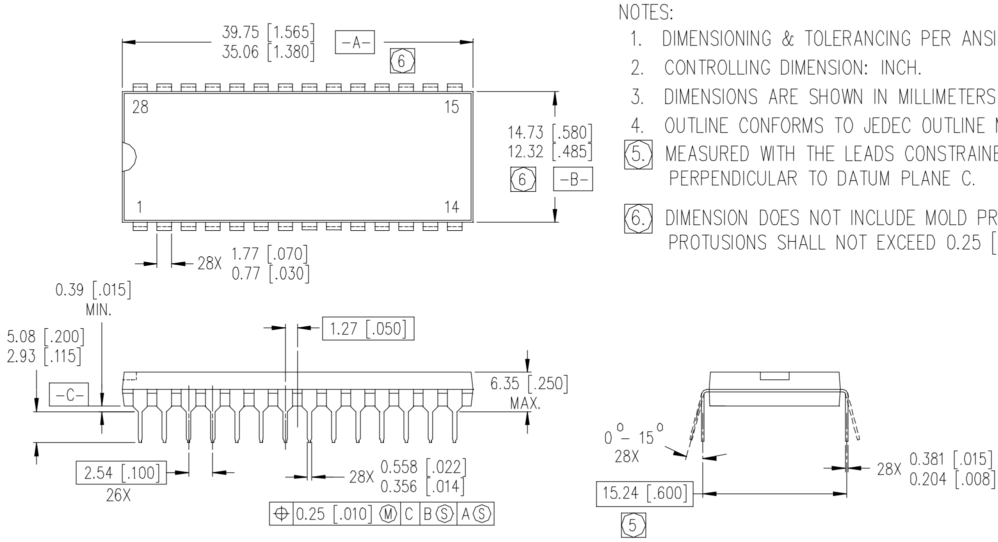


Figure 58. IR2130J/IR2132J
T_J vs. Frequency (IRGPC50KD2)
R_{GATE} = 10Ω, V_{CC} = 15V

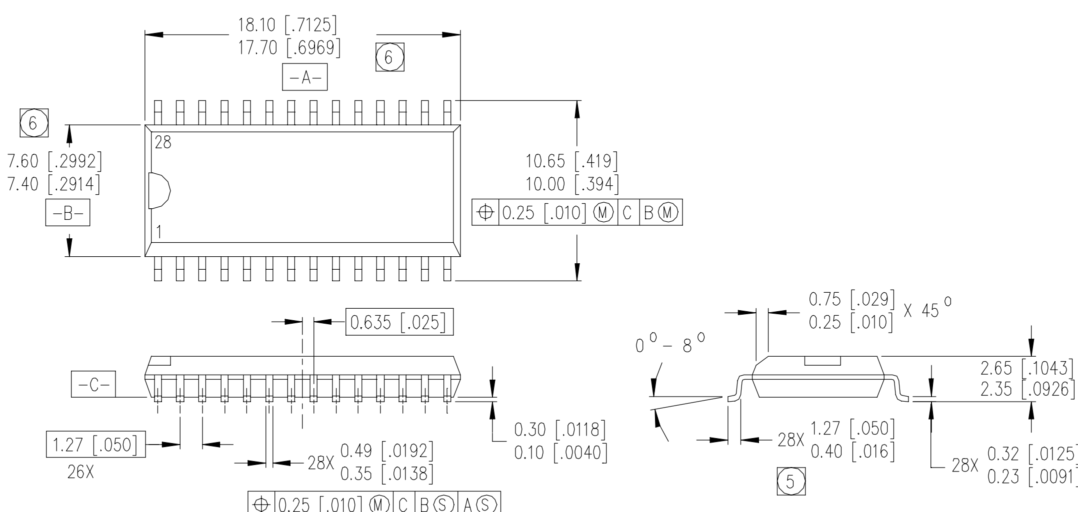
Case outlines

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)



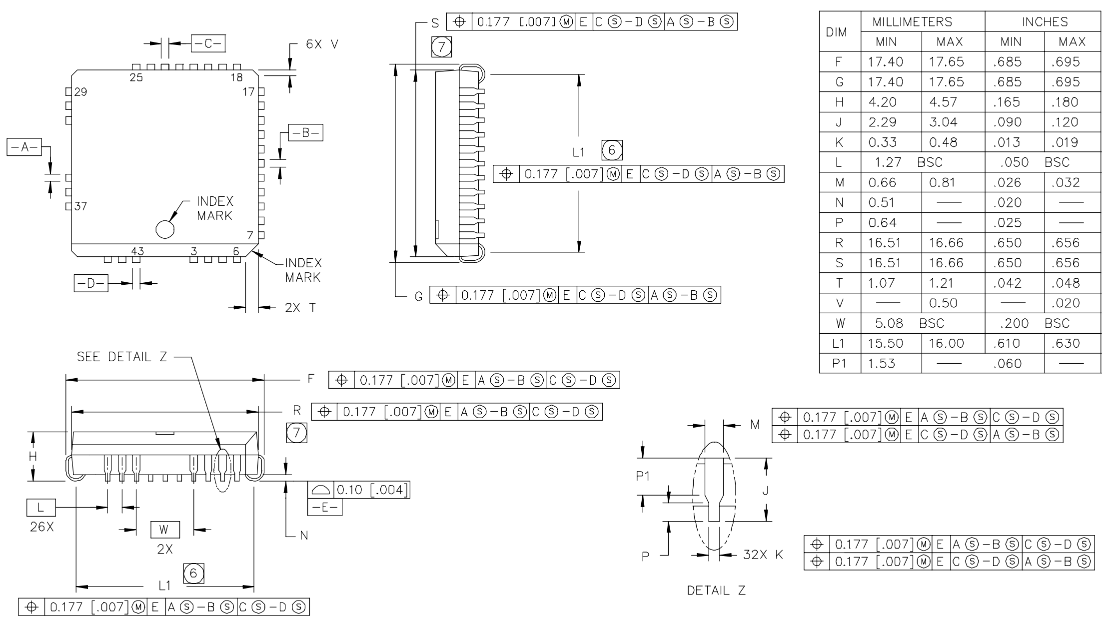
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-304002 (MS-013AE)

Case outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	——	.020	——
P	0.64	——	.025	——
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	——	0.50	——	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	——	.060	——

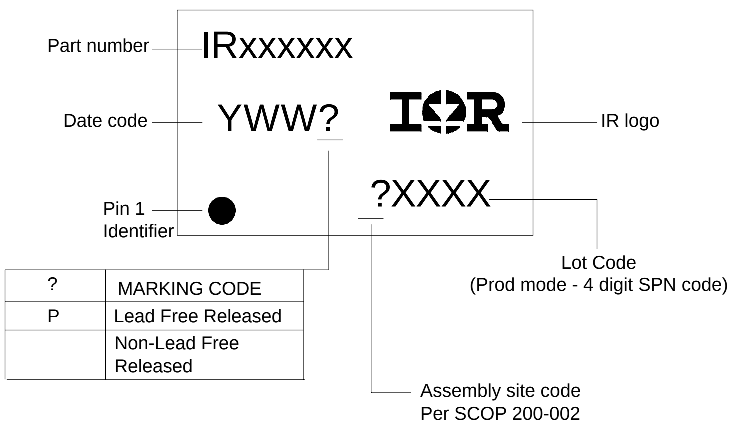
NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

28-Lead PDIP IR2130 order IR2130
28-Lead SOIC IR2130S order IR2130S
28-Lead PDIP IR2132 order IR2132
28-Lead SOIC IR2132S order IR2132S
44-Lead PLCC IR2130J order IR2130J
44-Lead PLCC IR2132J order IR2132J

Leadfree Part

28-Lead PDIP IR2130 order IR2130PbF
28-Lead SOIC IR2130S order IR2130SPbF
28-Lead PDIP IR2132 order IR2132PbF
28-Lead SOIC IR2132S order IR2132SPbF
44-Lead PLCC IR2130J order IR2130JPbF
44-Lead PLCC IR2132J order IR2132JPbF

International IOR Rectifier
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
This product has been qualified per industrial level
Data and specifications subject to change without notice. 4/2/2004